Electronic Version
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Claims

[c1] 1. A method of manufacturing a semiconductor device, comprising the steps of:
providing a substrate;
forming a mask layer over the substrate;
patterning the mask layer and the substrate to form a first opening in the substrate;
forming a gate dielectric layer, a first conductive layer and a second conductive layer inside the first opening sequentially, wherein the gate dielectric layer covers the interior surface of the first opening, the first conductive layer covers the gate dielectric layer and the second conductive layer completely fills the first opening;
removing a portion of the first conductive layer and the second conductive layer so that the upper surface of a remaining first conductive layer and a remaining second conductive layer in the opening are at a level slightly below the upper surface of the substrate and thereby form a second opening;
forming a cap layer inside the second opening;
removing the mask layer; and
forming a source/drain region in the substrate.

[c2] 2. The method of claim 1, wherein the step of forming the source/drain region is performed after the step of removing the mask layer.

[c3] 3. The method of claim 1, wherein the step of forming the source/drain region in the substrate is performed before the step of forming the mask layer over the substrate.

[c4] 4. The method of claim 3, further comprises a step of forming a well region in the substrate before the step of forming source/drain region in the substrate.

[c5] 5. The method of claim 4, wherein the step of forming the source/drain region and the step of forming the well region in the substrate use the same layer as a implanting mask.

[c6] 6. The method of claim 1, further comprises a step of forming a well region in the substrate before the step of forming the mask layer on the substrate.

[c7] 7. The method of claim 1, wherein after the step of forming a mask layer over the substrate, furthermore comprises forming a bottom anti-reflection layer over the mask layer; and the step of patterning the mask layer and the substrate to form a first opening furthermore comprises patterning the bottom anti-reflection layer.

[c8] 8. The method of claim 1, wherein the first conductive layer comprises a polysilicon layer.

[c9] 9. The method of claim 1, wherein the second conductive layer comprises a refractory metal silicide layer.

[c10] 10. The method of claim 9, wherein material constituting the refractory metal silicide layer is selected from a group consisting of tungsten silicide, nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, platinum silicide and palladium silicide.

[c11] 11. The method of claim 1, wherein the step of removing a portion of the first conductive layer and the second conductive layer comprises:
performing a chemical-mechanical polishing process to remove portions of the first conductive layer and the second conductive layer outside the opening; and
etching back the first conductive layer and the second conductive layer in the opening so that the upper surface of the remaining first conductive layer and the remaining second conductive layer in the opening are at a level slightly below the upper surface of the substrate and thereby form a second opening.

[c12] 12. The method of claim 1, wherein the mask layer is fabricated using a material having an etching selectivity

that differs from the material constituting the first conductive layer, the second conductive layer and the cap layer.

[c13] 13. The method of claim 1, wherein after the step of patterning the mask layer and the substrate to form the opening further comprises performing a threshold voltage adjustment process.

[c14] 14. The method of claim 1,further comprising:
forming an inter-layer dielectric layer over the substrate; and
forming a contact opening in the inter-layer dielectric layer using the cap layer as a self-aligned mask.

[c15] 15. A semiconductor device, comprising:
a substrate having an opening therein;
a dielectric layer formed on the interior surface of the opening;
a first conductive layer formed on the dielectric layer inside the opening;
a second conductive layer formed over the first conductive layer and filled the opening entirely;
a cap layer formed over the first conductive layer and the second conductive layer; and
a source/drain region formed in the substrate on each side of the second conductive layer.

[c16] 16. The semiconductor device of claim 15, wherein the first conductive layer has a U-shaped cross-sectional profile.

[c17] 17. The semiconductor device of claim 15, wherein the second conductive layer comprises a refractory metallic silicide layer.

[c18] 18. The semiconductor device of claim 15, wherein the first conductive layer comprises a doped polysilicon layer.

[c19] 19. The semiconductor device of claim 15, wherein the junction of the source/drain region is set at a level higher than a bottom of the opening.

[c20] 20. The semiconductor device of claim 15, wherein the junction of the source/drain region is set at a level slightly lower than a bottom of the opening.

[c21] 21. The semiconductor device of claim 15, wherein the device furthermore comprises a well region in the sub-strate.

[c22] 22. The semiconductor device of claim 15, wherein the junction of the source/drain region is at a level higher than a bottom of the polycide gate structure.

[c23] 23. The semiconductor device of claim 15, wherein the junction of the source/drain region is at a level slightly lower than a bottom of the polycide gate structure.